***EE/CprE/SE 492 BIWEEKLY REPORT 01***

**Date:** September 1, 2022 – September 16, 2022

**Group number:**  Dec2022-20

**Project title:** i281 CPU Hardware Implementation

**Client &/Advisor:** Dr. Alexander Stoytchev

**Team Members/Role:**

Alex Keifer (Hardware Team)

David Vachlon (Software Team)

Joseph De Jong (Hardware Team)

Saffron Edwards (Software Team)

Patrick O’Brien (Hardware Team)

**Summary**

This week consisted of our first meeting of the semester with Professor Stoytchev. We met up with him to discuss the overall project, and the remaining components that need to get done. After the meeting we placed an order for the remaining parts needed for the project, and delegated tasks to each team member. We worked on creating and debugging a crystal oscillator circuit for the clock module, which will provide a 1MHz clock signal to the rest of our components. We also discussed methods of programming our instruction and data memory modules using EEPROM and SRAM chips and how the software to hardware interface will possibly work.

**Past Week Accomplishments**

* **Alex Kiefer:** Worked with Patrick to create a crystal oscillator clock module. Several designs were built and tested, with the winning design showing better characteristics.
* **David Vachlon:** Researched communication protocols to interface with the final computer. Talked with the professor regarding the details of the boot sequence.
* **Joseph De Jong:** Designed a single graphics processor memory module. This device will be used 8 times in the graphics processor to create a working output.
* **Saffron Edwards:** Discussed potential software solutions with David regarding the interface with hardware components.
* **Patrick O’Brien:** Worked with Alex to create a crystal oscillator clock module. Several designs were built and tested, with the winning design showing better characteristics. Soldered the surface mount EEPROM chips onto breakout boards.

**Pending Issues**

* **David Vachlon:** Needs to finalize the interface between the software and hardware components. Need to purchase a set of seven-segment displays and other discussed chips.
* **Joseph De Jong:** Originally, created a set of 2-1 bus multiplexores to be used throughout the system. However, 5 additional bus multiplexores will be required. Will also need to design, purchase and build these additional multiplexores for the team.
* **Patrick O’Brien:** Needs to redesign the Arduino EEPROM programmer to work with the new EEPROMs that were purchased. This will require expanding the number of address spots on the breadboard and in the code.

**Individual Contributions**

| **NAME** | **Individual Contributions** | **Hours this**  **week** | **HOURS**  **cumulative** |
| --- | --- | --- | --- |
| Alex Kiefer | Clock Module Breadboarding, created program counter. | 5 | 10 |
| David Vachlon | Parts Ordering, Researched Software Component | 5 | 10 |
| Joseph De Jong | Parts Listing, Detailed Meeting Notes, Designed GPU Memory | 5 | 10 |
| Saffron Edwards | Helped discuss ideas for software component | 2.5 | 5 |
| Patrick O’Brien | EEPROM SMD Soldering, Clock Module Breadboarding | 5 | 10 |

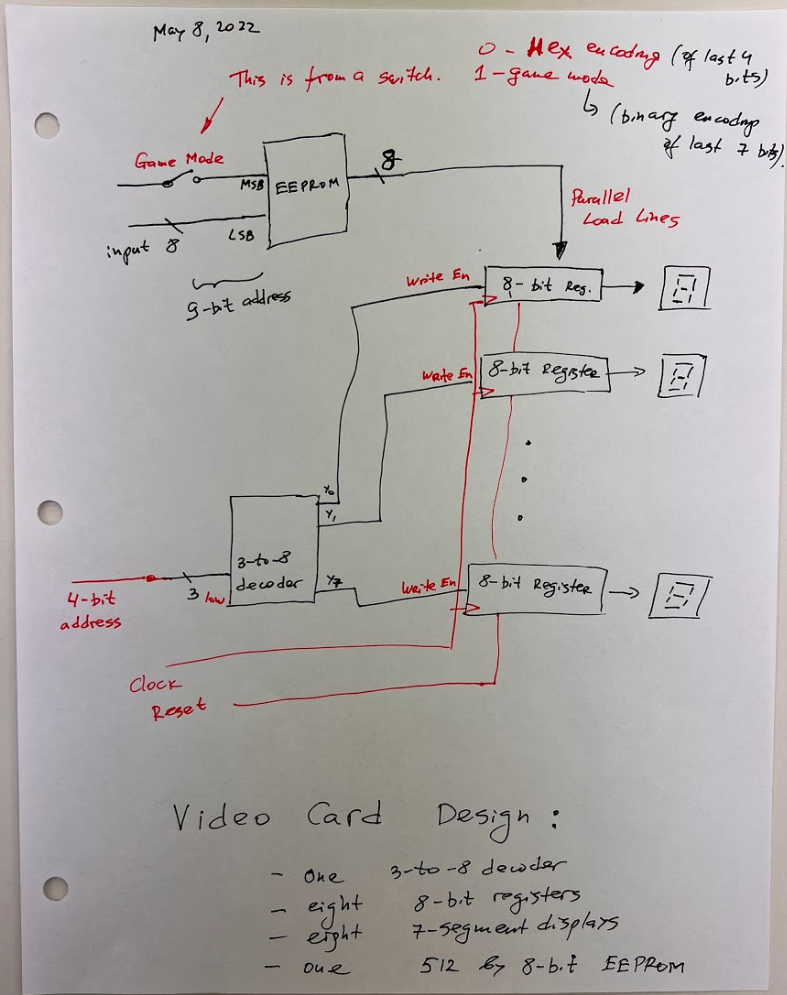
**Plans for the Coming Week**

* **Alex Kiefer:** Work on the construction of the instruction memory module.
* **David Vachlon:** Order any outstanding parts. Work with the hardware to develop the video card. Continue to develop an interface between hardware and software.
* **Joseph De Jong:** Build the storage for the video card. The storage will consist of 8x 8-bit registers used to control a set of graphical outputs (7-seg. displays). Each storage register will include a reset, write enable, clock and bus access. After completion of the storage, the EEPROM will need to be programmed for normal function and game mode.
* **Saffron Edwards:** Work with David Vachlon to develop the interface between software and hardware.
* **Patrick O’Brien:** Work on redesigning the EEPROM programmer, and then work with other team members to program the new EEPROM chips with the boot sequence and video card decoding.

**Summary of Weekly Advisor Meeting**

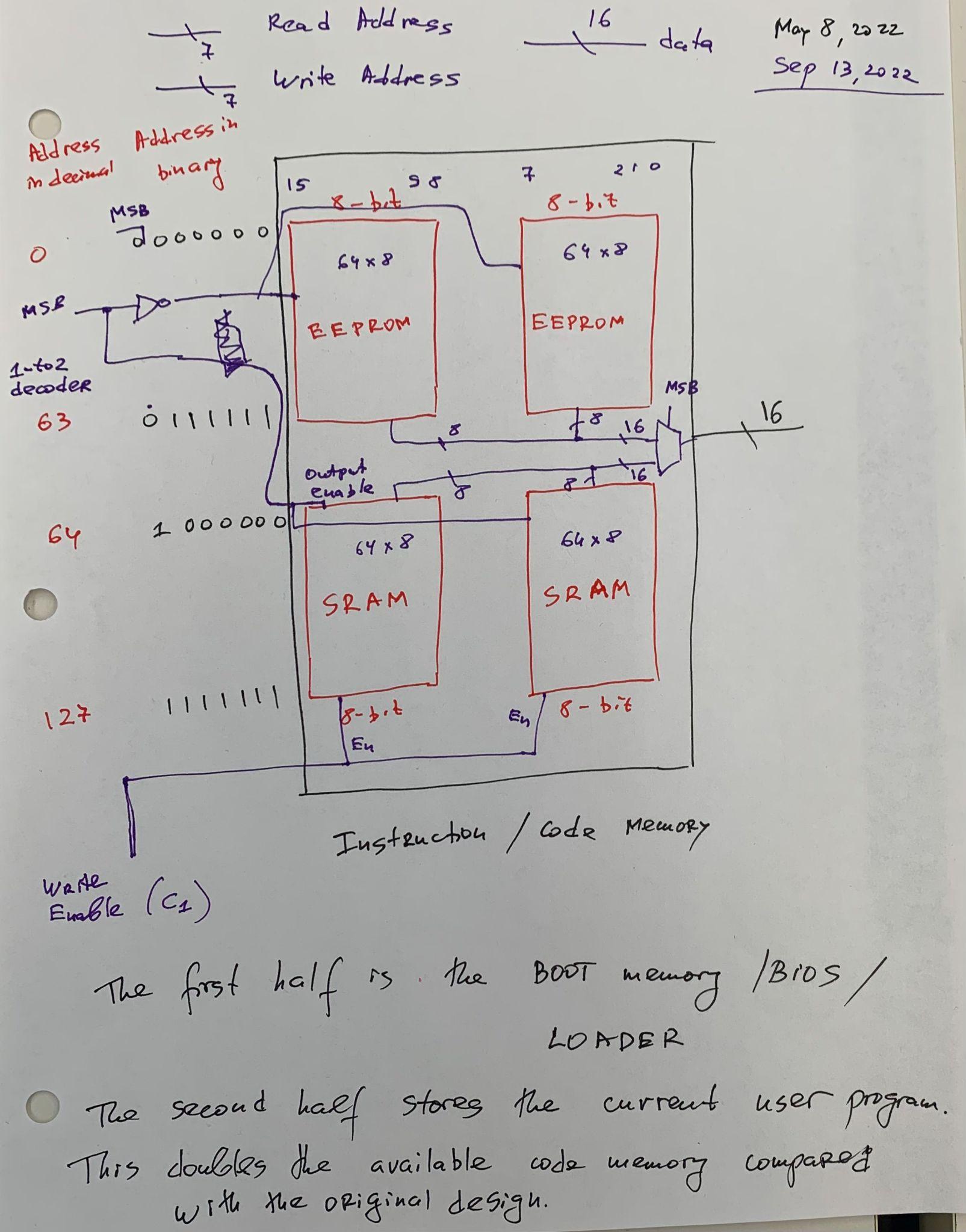
Our meeting with Professor Stoytchev focused on getting us up to date with the project, since we had not had access to it over the summer. Some of the lingering questions that we had regarding the project involved the instruction memory, data memory, and “video card”. We had concerns over the original plan for the video card, because it required wiring an 8-bit, 4 to 16 decoder on breadboards, requiring many connections and a very high margin of errors occurring. We discussed the issue with Professor Stoytchev, and decided that using EEPROM chips as the decoders would require much less wiring, and would save space on the final board.

***Graphics Processor:***

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Another issue that we left for the summer with, was how exactly to handle the boot sequence required to initialize the computer. With Professor Stoytchev’s assistance, we were able to figure out a theoretical solution to the issue, shown in the figure below, but haven’t yet tested the solution. We determined that creating a massive lookup table on a set of EEPROM chips would cover any possible input of variables, and would output the correct control signals to the computer. By using the 1MHz clock module that was created this week, the boot sequence would only take a fraction of a second to complete.

***Instruction Memory Boot Sequence:***

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